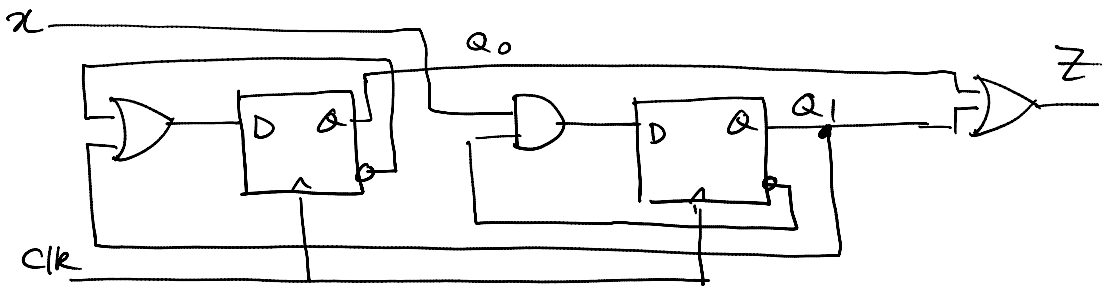
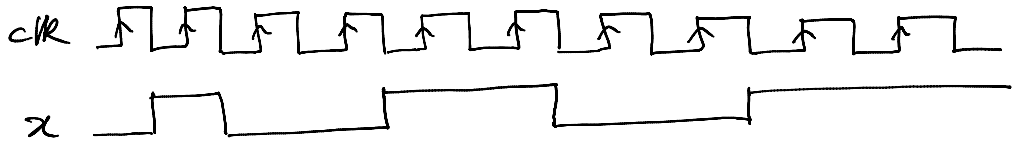
EE365 HW #4

1. Analyze the clocked synchronous state machine shown below. Write excitation equations, excitation/transition table, and statte/output table. Initial state Q1Q0 = 00. (Source: Digital Design by John Wakerley)



2. Draw the timing diagram of the output z of problem 1 for the input x shown as below.



3. Swap AND and OR gates in prob1 and repeat the analysis.
4. Draw the timing diagram of the output z of problem 2 for the input x shown in problem 2.
5. Design a counter with an active low enable En_L and the following sequence (and repeats itself)